a reset terminal for receiving an external power-on reset signal; and

C2 a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.

Sub D1 5. (Twice Amended) A semiconductor integrated circuit comprising:

C3 a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

C4 Sub D1 7. (Twice Amended) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

Sub D1 C5 8. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator, including transistors having threshold values, for generating a plurality of sub power-on reset signals on basis of the respective threshold

values of each of the transistors; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signals.

9. (Amended) A semiconductor integrated circuit comprising:

a first sub reset signal generator, including a first transistor having a first threshold voltage, for generating a first sub power-on reset signal on basis of the first threshold voltage;

C5 cont.

a second sub reset signal generator, including a second transistor having a second threshold value, for generating a second sub power-on reset signal on basis of the second threshold voltage; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of the first sub power-on reset signal and the second sub power-on reset signal.

10. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a plurality of pulse generators for generating pulses on basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

11. (Amended) A method of initializing a semiconductor integrated circuit having a sub reset signal generator including transistors having threshold values, the method comprising the steps of:

C5

generating a plurality of sub power-on reset signals, each according to ~~a~~ respective threshold values of each of the transistors;

generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one of said power-on reset signals.

14. (Amended) A semiconductor integrated circuit according to claim 13, wherein said main reset signal generator comprises:

C6

Sub D1

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

16. (Amended) A semiconductor integrated circuit according to claim 15, wherein said main reset signal generator comprises:

C7

Sub D1

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on

reset signal.

Please add new claims 18-20 as follows:

-- 18. (New) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a main power-on reset signal to initialize an internal circuit, according to at least one of said plurality of sub power-on reset signals, wherein

said main reset signal generator generates said main power-on reset signal having pulses respectively corresponding to each of said sub power-on reset signals, when threshold values of transistors formed in said semiconductor integrated circuit are typical values.

19. (New) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of said semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to one of said sub power-on reset signal and said external power-on reset signal.

20. (New) A method of initializing a semiconductor integrated circuit having a sub reset signal generator including transistors having threshold values, the method comprising the steps of: